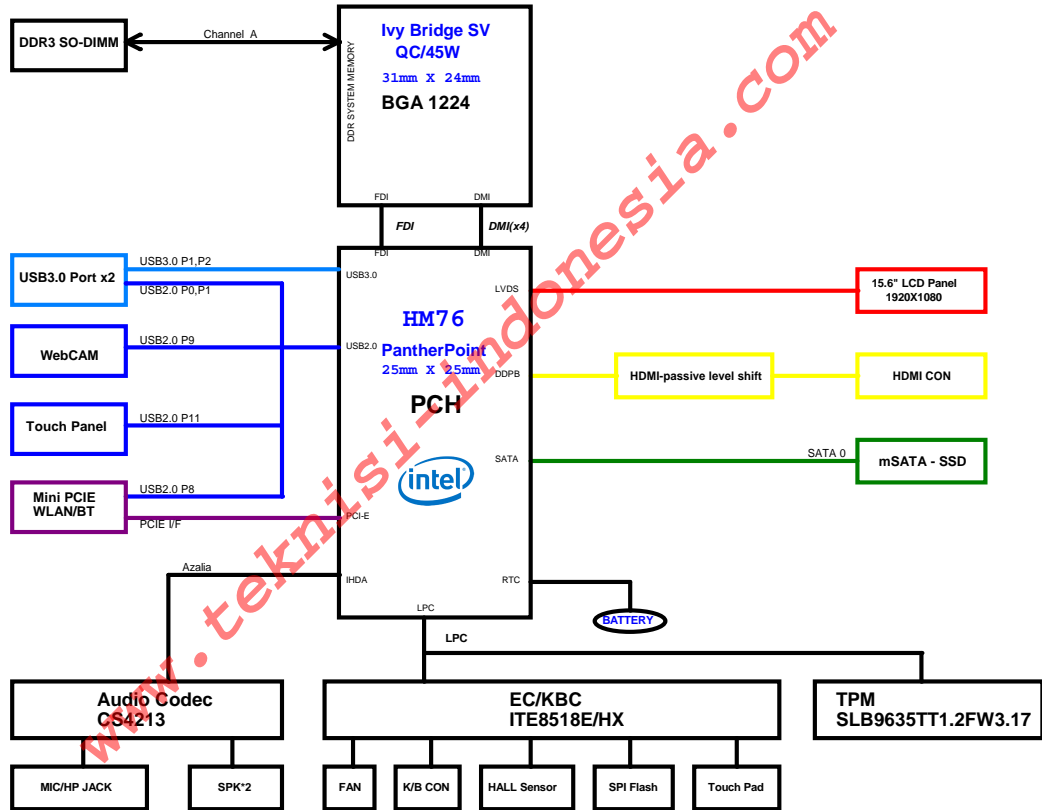


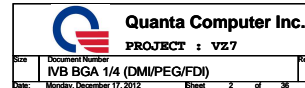
PCB 8 Stackups

LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : IN3
 LAYER 7 : GND
 LAYER 8 : BOT

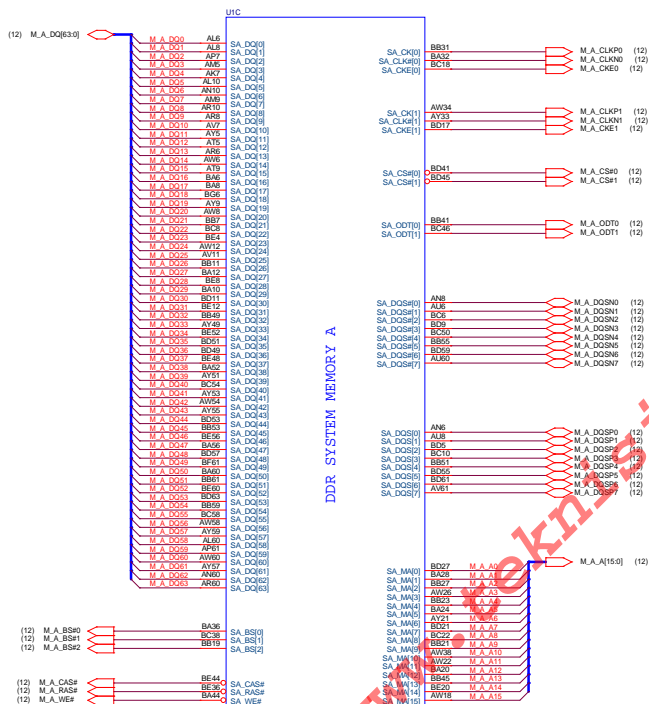
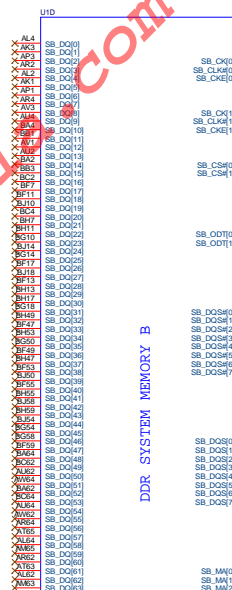
VZ7 14 inch Block Diagram



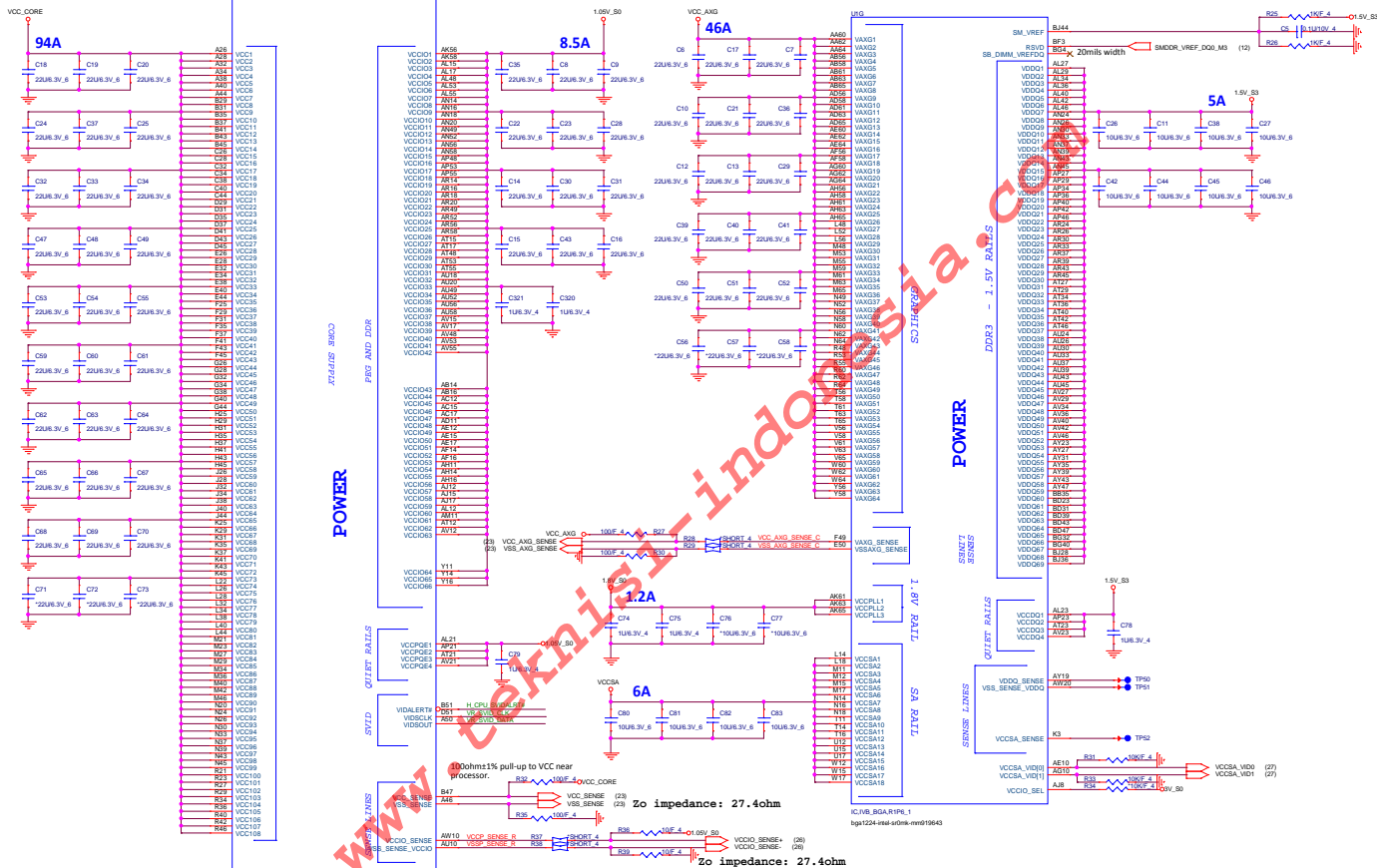
FEG_COMF connect to FIN GT W. 12mm/S. 15mm/S. 50mm/S



Ivy Bridge Processor (DDR3)

IC,IVB_BGA_R1P6_1
bga1224-intel-s20mk-mm919642

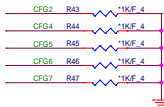
IC,NB_BGA_R1P6_1
bga1224-intel-sr0mk-mm919641

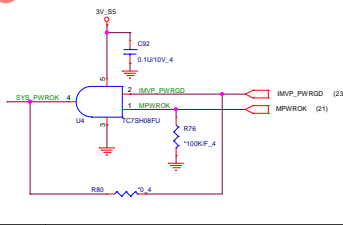
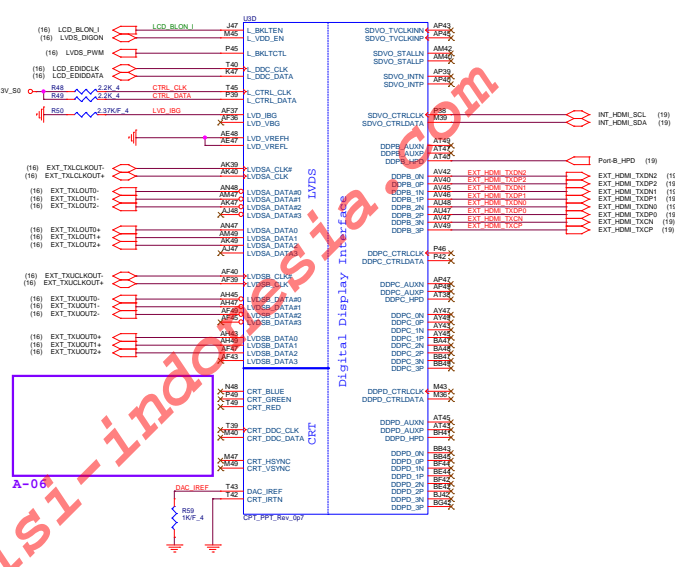


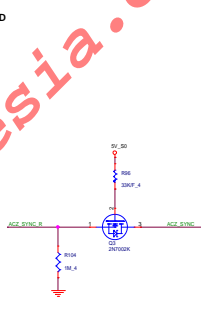
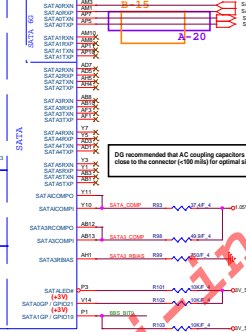
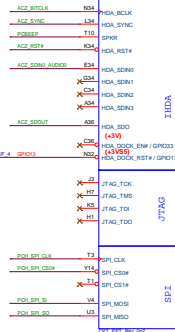
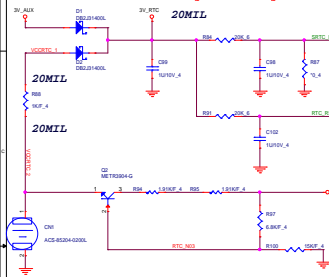


Processor Strapping

CFG2	0	PCIe X16 LANE Reversed
	1	Normal Operation
CFG3	0	PCIe X4 LANE Reversed
	1	Normal Operation
CFG4	0	Enable; An ext DP device is connected to eDP
	1	Disable; No physical DP attached to eDP
CFG(5:6)	00	1 x 8, 2 x 4 PCIe
	01	Reserve
	10	2 x 8 PCIe
	11	1 x 16 PCIe
CFG7	0	PEG Wait for BIOS for training
	1	PEG Train immediately following PLT_RST#





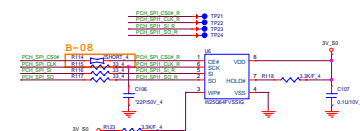


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Intelcore	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>CONF1</th><th>CONF2</th><th>Boot Location</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>BIOS</td></tr><tr><td>1</td><td>0</td><td>LPC</td></tr></tbody></table>	CONF1	CONF2	Boot Location	0	0	BIOS	1	0	LPC	
CONF1	CONF2	Boot Location											
0	0	BIOS											
1	0	LPC											
GPIO19	Different from Capella	PWROK	Should not be pull-down (weak pull-up 20K)										
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Thief HDD protection Only for Intelcore	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-the PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO6	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28	On-the PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SP1_MOS1	iTPM function Disable	APWROK	0 = Enable (weak pull-down 20K) 1 = Enable										

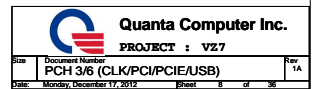
PCH Dual SPI BIOS & ME F/W ROM 8MB



HDA Bus



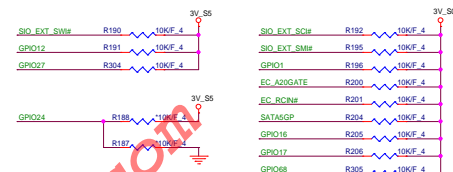
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



+3V SS/AD0 / GPIO38	NC_1	P37
+3V SSA/ROUT0 / GPIO39		
+3V SSA/ROUT1 / GPIO48	VSS_NC1F_15	BC22
+3V SATAPG / GPIO49 / TEMP_ALERT	VSS_NC1F_16	BC45
+3V GPIO57 +3V_SS	VSS_NC1F_17	BL13
	VSS_NC1F_18	BL47
	VSS_NC1F_19	BL44
	VSS_NC1F_20	BL44
	VSS_NC1F_21	BL45
	VSS_NC1F_22	BL46
	VSS_NC1F_23	BL46
	VSS_NC1F_24	BL6
	VSS_NC1F_25	C2
	VSS_NC1F_26	C48
	VSS_NC1F_27	D1
	VSS_NC1F_28	D48
	VSS_NC1F_29	E1
	VSS_NC1F_30	F49
	VSS_NC1F_31	F49
	VSS_NC1F_32	F49
QPI_PPT_Rev.5p7		



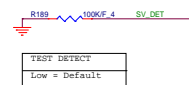
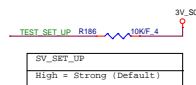
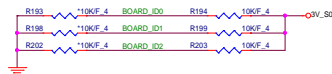
09



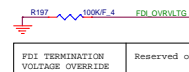
		VZ7-TOUCH	VZ7-NON TOUCH	VZ8-TOUCH	VZ8-NON TOUCH
BOARD ID0	GPIO69	HIGH	HIGH	LOW	LOW
BOARD ID1	GPIO39	HIGH	LOW	LOW	HIGH

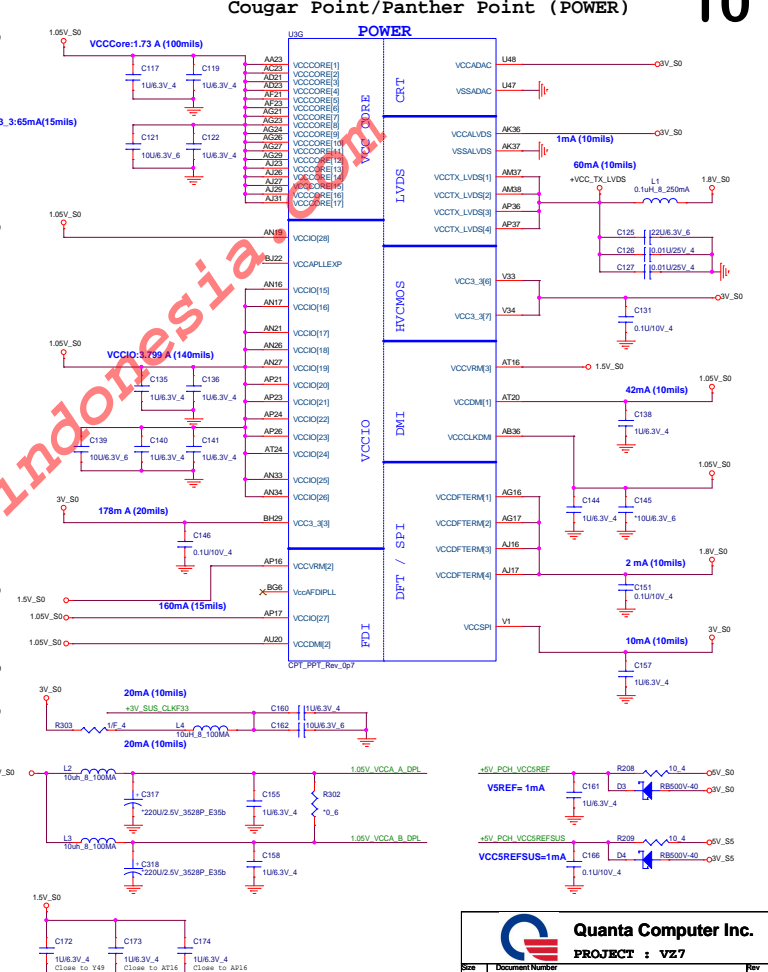
		VZ7-TOUCH	VZ7-NON TOUCH	VZ8-TOUCH	VZ8-NON TOUCH
BOARD_ID0	GPIO69	HIGH	HIGH	LOW	LOW
BOARD_ID1	GPIO39	HIGH	LOW	LOW	HIGH

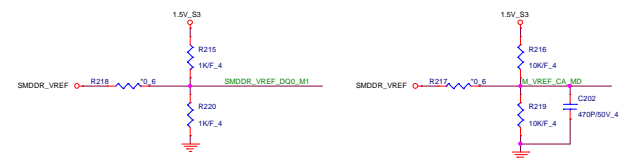
		SSD-HDD	SATA-HDD
BOARD ID2	GPIO36	HIGH	LOW

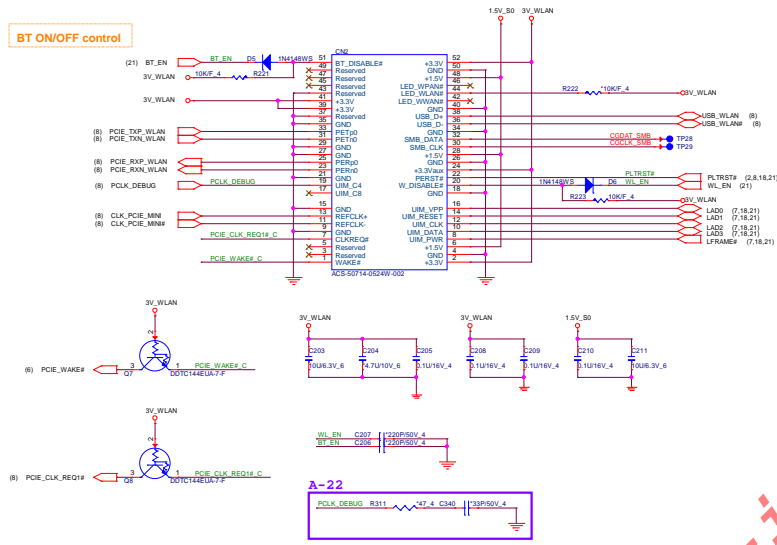


MFG-TEST



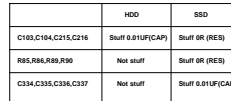






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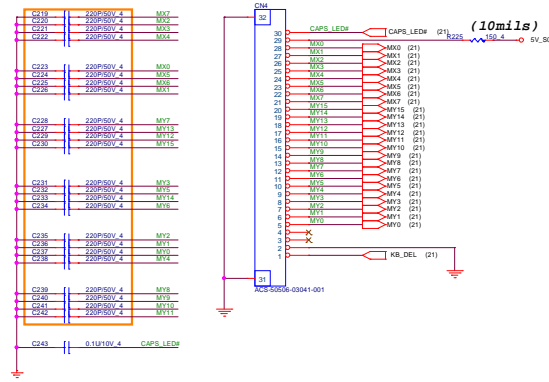
14

[illegible]

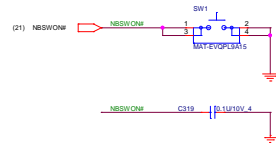
B-07 B-13

INT KeyBoard

B-14



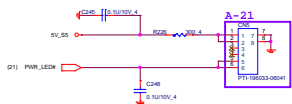
PWR SW Bottom



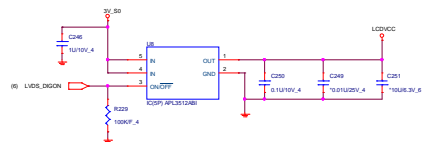
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LED

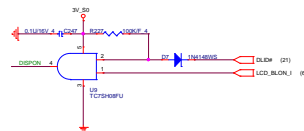
0.2A(20mils)



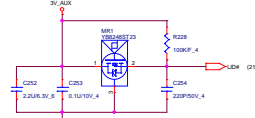
LCD POWER SWITCH



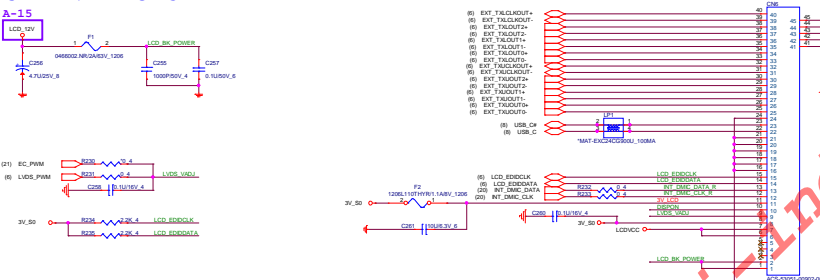
PANEL BACKLIGHT CONTROL



HALL SENSOR



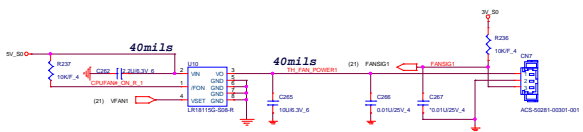
LCD PANEL MODULE



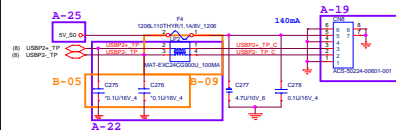
For EMI close to connector



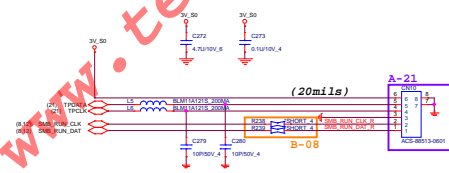
FAN CONNECTOR



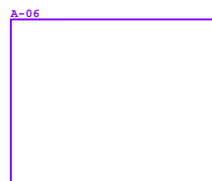
TOUCH MODULE

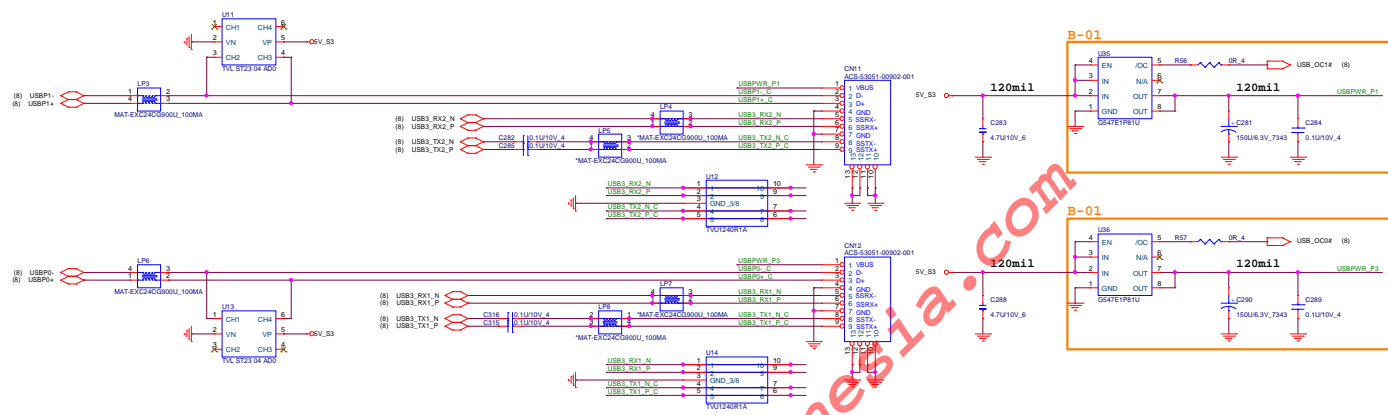


TP BOARD



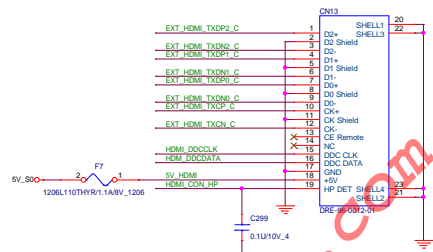
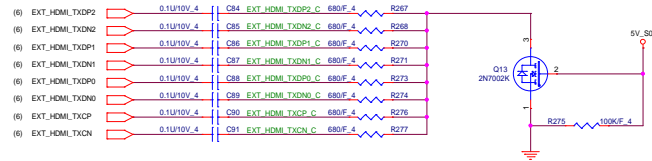
CRT DEBUG





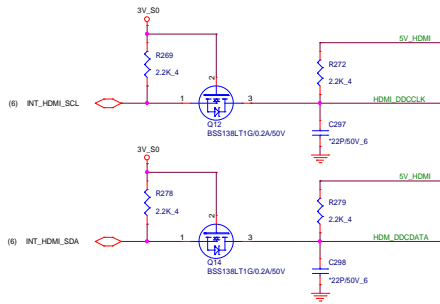
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HDMI CONNECTOR

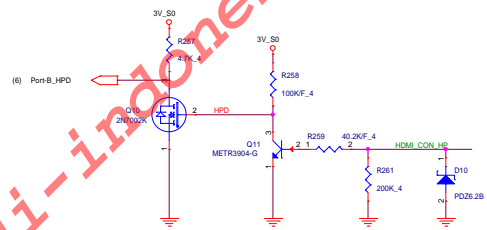


HDMI-OUT PORT

DDC Level Shift



HPD



EMI

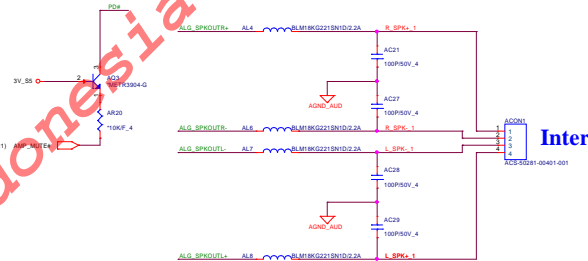
EXT_HDMI_TXCN_C	R263	120F_4	EXT_HDMI_TXCP_C	A-22
EXT_HDMI_TXDN2_C	R264	120F_4	EXT_HDMI_TXDP2_C	
EXT_HDMI_TXDN1_C	R265	120F_4	EXT_HDMI_TXDP1_C	
EXT_HDMI_TXDN0_C	R266	120F_4	EXT_HDMI_TXDP0_C	



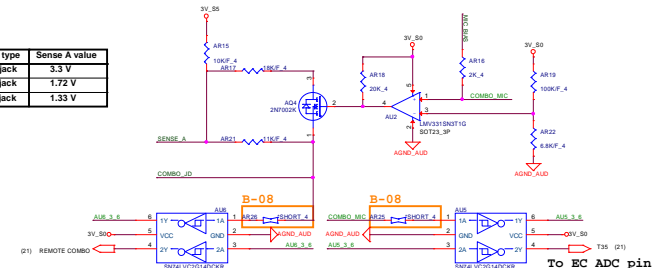
3x MIC_BIA
6x GND
1x ALG_HP_1
2x ALG_HP_2
4x GND
5x ALG_HP_3

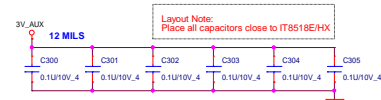
3	MIC_BIAS
6	GND
1	ALG_HP_L
2	ALG_HP_R
4	GND
5	ALG_HP_SENSE

Internal SPK

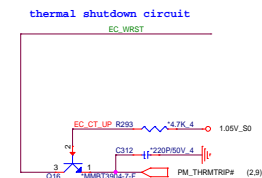


Jack type	Sense A value
Non-jack	3.3 V
Normal jack	1.72 V
Combo jack	1.33 V






For Battery charge/Therm2
For PCH SMB/DDR Thermal IC
/VGA/Audio DSP

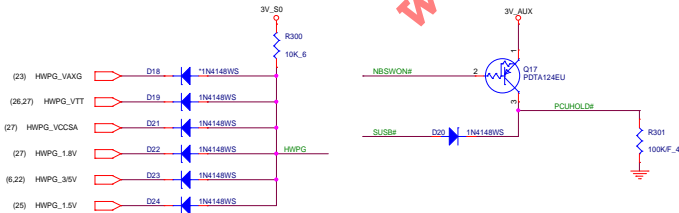


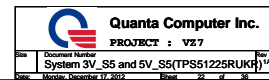
0.025A(20mils)



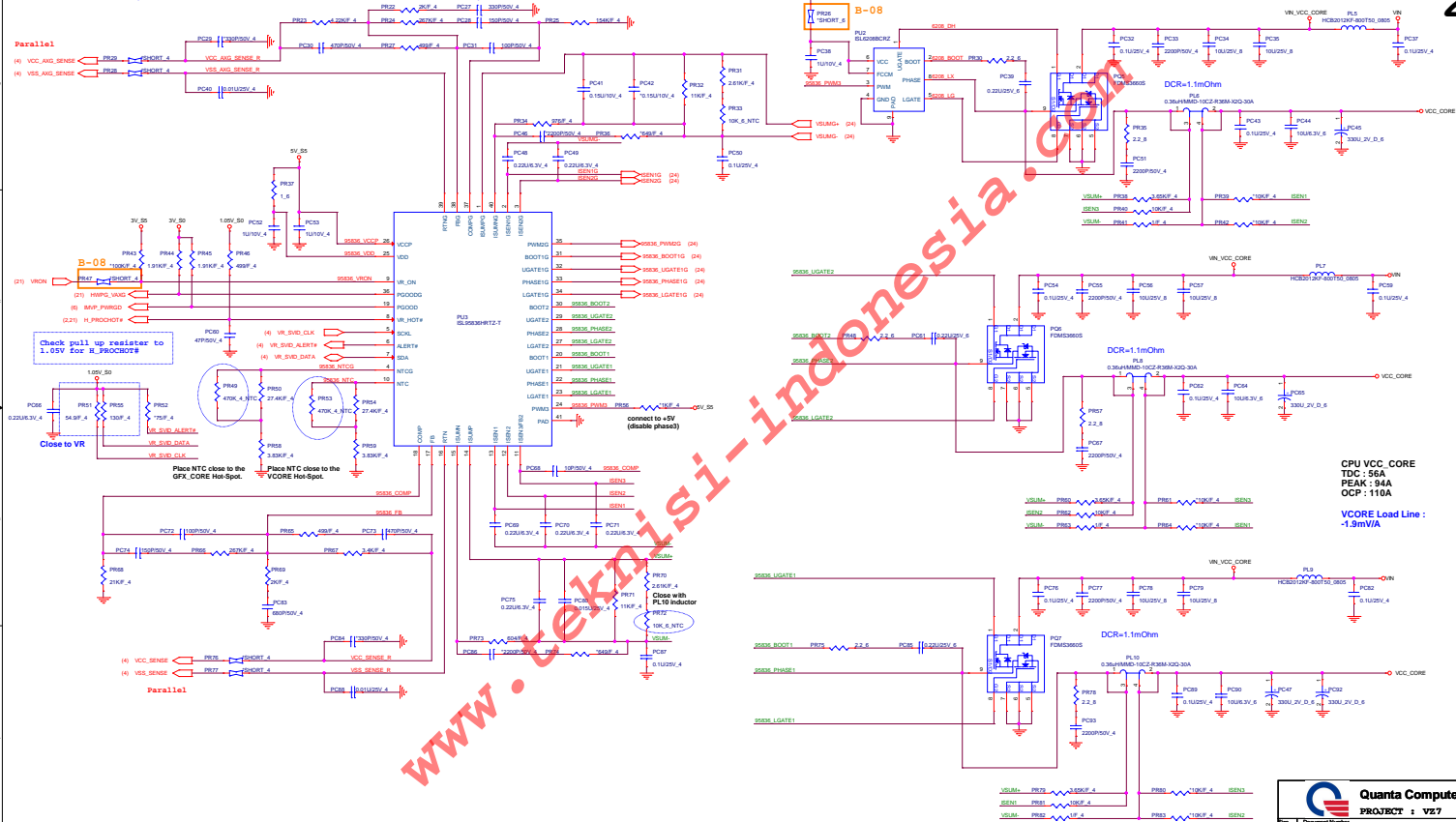
 Quanta Computer Inc. PROJECT : VZ7	
Size	Document Number EC_ITE8518E/HX
Date	Monday, December 17, 2013
Sheet	24 of 36

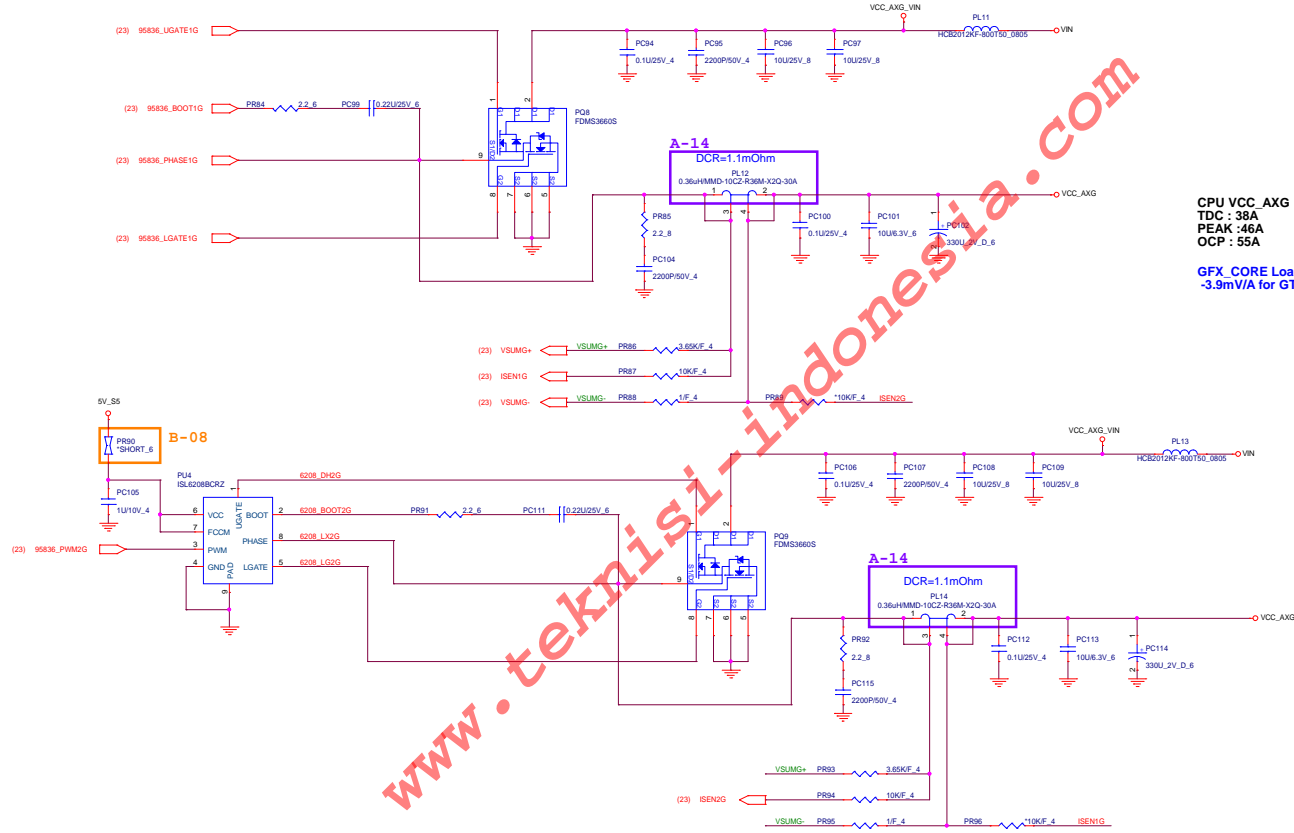
(23)	HWPQ_VAXG	D18	*1N4148WS
(26,27)	HWPQ_VTT	D19	*1N4148WS
(27)	HWPQ_VCCSA	D21	*1N4148WS
(27)	HWPQ_1.8V	D22	*1N4148WS
(6,22)	HWPQ_35V	D23	*1N4148WS
(25)	HWPQ_1.5V	D24	*1N4148WS





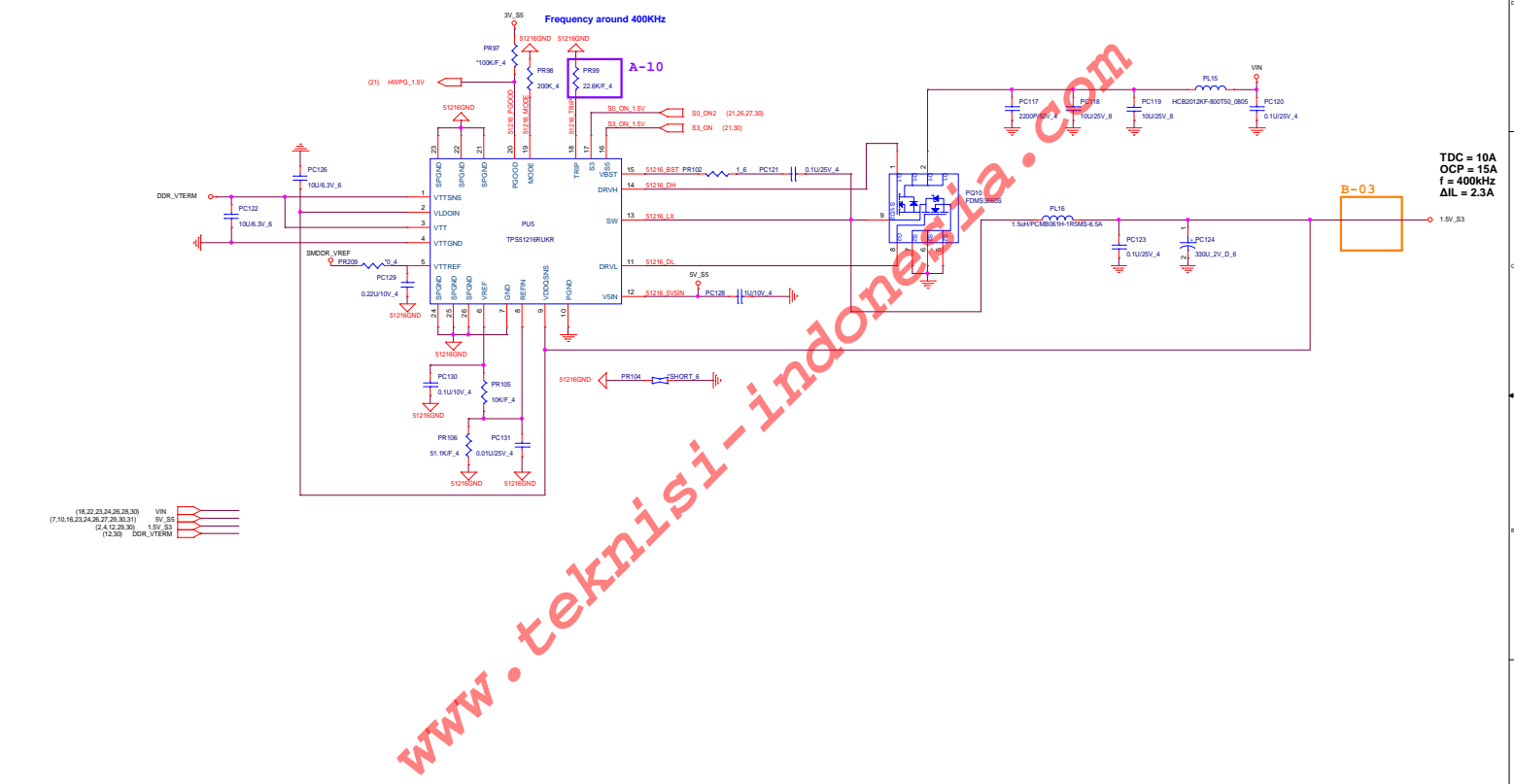
CPU VCORE (ISL95836HRTZ-T and ISL6208CRZ-T)





CPU VCC_AXG
TDC : 38A
PEAK : 46A
OCP : 55A

GFx_CORE Load Line :
-3.9mV/A for GT2

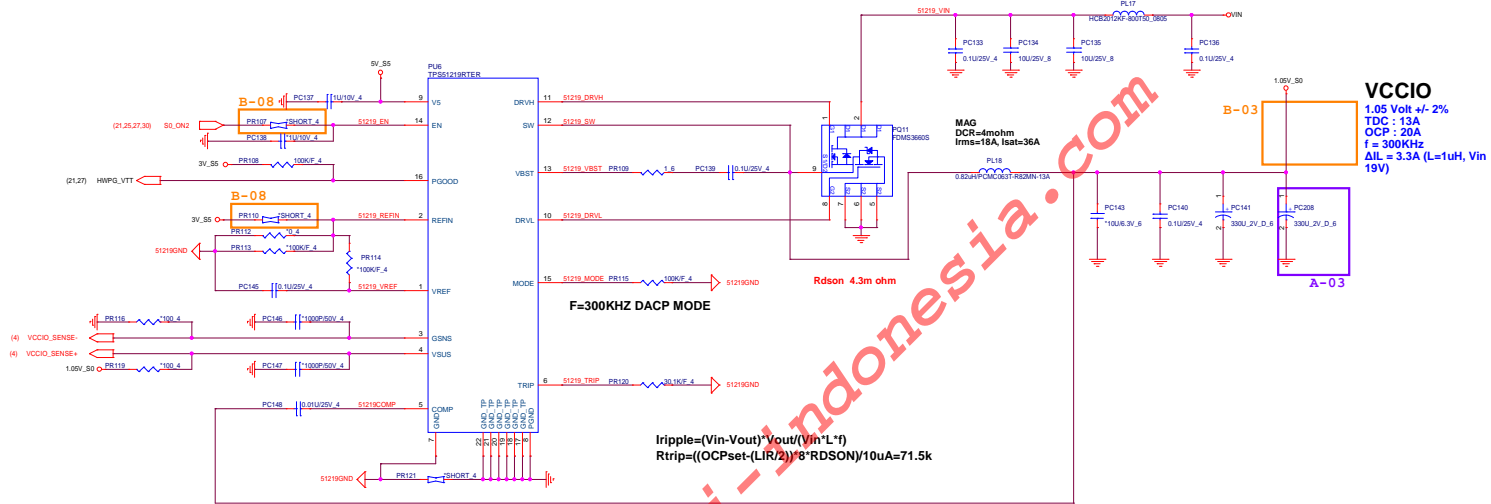


(18,22,23,24,26,28,30) VIN
(17,10,16,23,24,26,27,29,30,31) 0V_SS
(2,4,12,28,30) 1.5V_S3
(12,30) DDR_VTERM

TDC = 10A
OCP = 15A
f = 400KHz
ΔIL = 2.3A

B-03

$I_{ripple} = (V_{in} - V_{out}) \cdot V_{out} / (V_{in} \cdot L \cdot f)$
R_TRIPa = $(1 \text{ lim}(22A) - 3.45A/2) \cdot 4.7 \text{ (mohm)} / 10u$
O.C.P setup information $\approx 9.53K \text{ (ohm)} \rightarrow (PR234)$



Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-1010MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG	CV-1010MZ00	21	30	3.1m Max.	11X10X4

$$V_{cs}(mV) = R_{cs}(K) \times 10 \mu A / 10$$

$$I_{ripple} = (V_{in} - V_{out}) \times V_{out} / (V_{in} \times L \times f)$$

$$\text{Current limit} = V_{cs}(mV) / R_{dson}(m) + I_{ripple} / 2$$

O.C.P setup information

Output	Mos Rds_on	I_OCP	DC ΔIL(A)	Freq(KHz)	Inductor	
1.05V	4.3m Max	25	3.97	300	1uH	100K

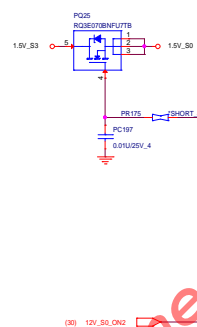
1.8V_S0 +/- 5%
Continue current:4A
Peak current:6A
OCP minimum:7A

1.8V_S0 +/- 5%
Continue current:1.48A

$V_{out} = 0.8 * (1 + R1/R2) = 1.817V$

REGN MAX voltage 6.5V
 $V_{ILIM}=20*(VSRP-VSRN)=20*I_{chg}*R_{sr}$
 =0.793V for 3.965A current limit

S0 ON2 Load SW



A-11

3V.55

PC208
AC94M

3V_1WLAN

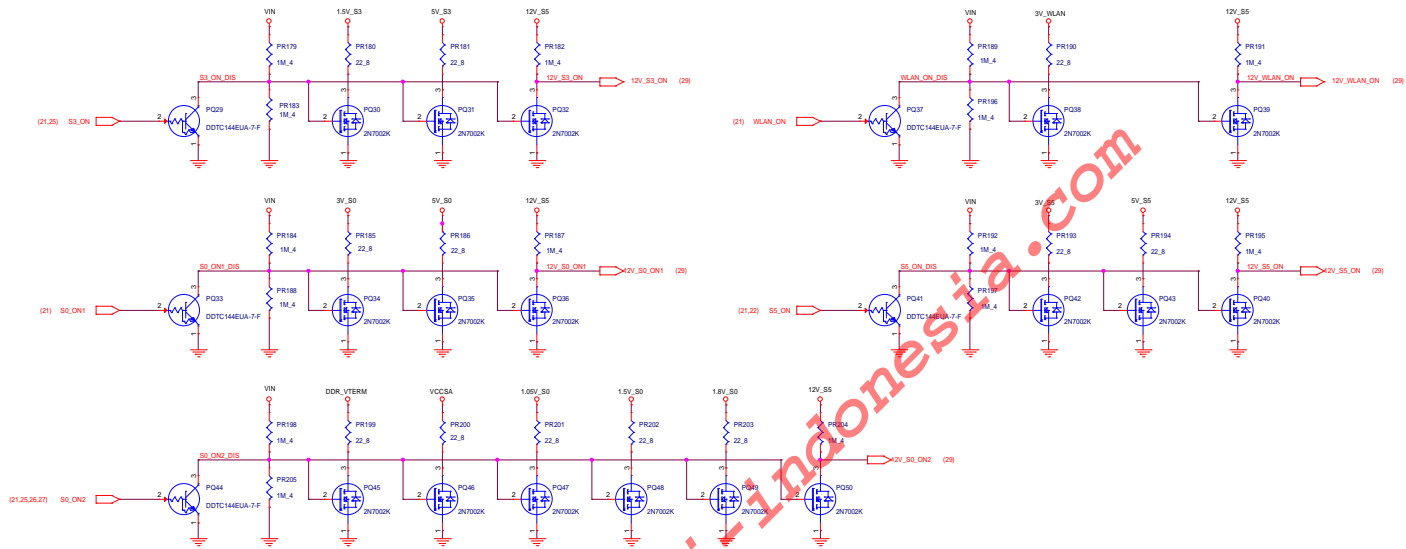
PS175

SHORT_4

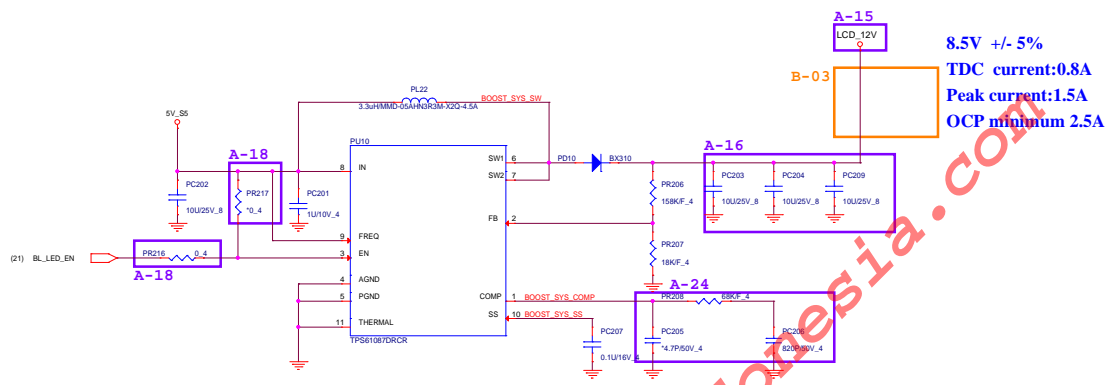
PC200

0.01u25V_4

3V_1WLAN ON

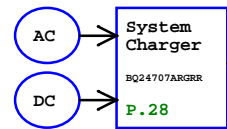


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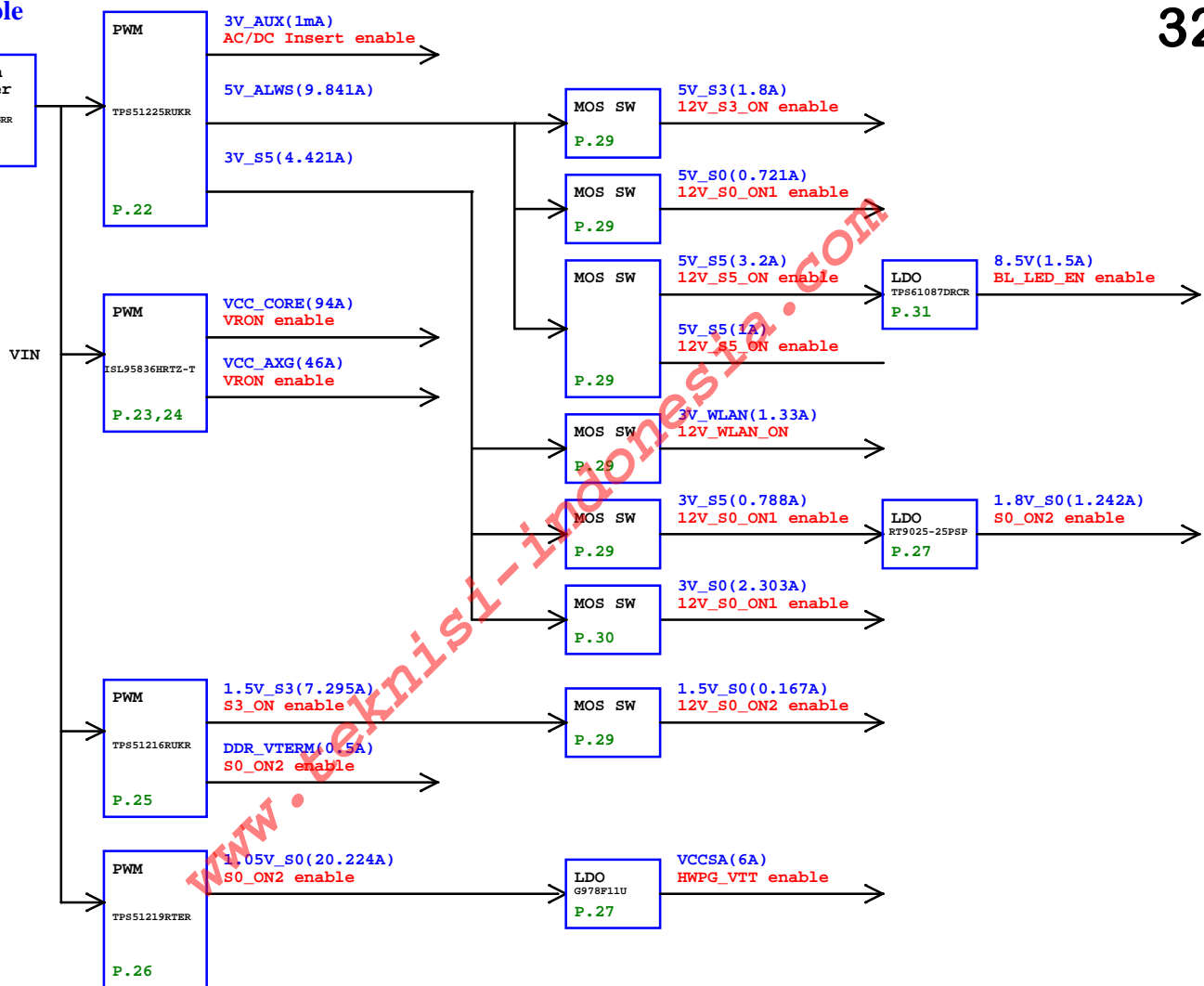


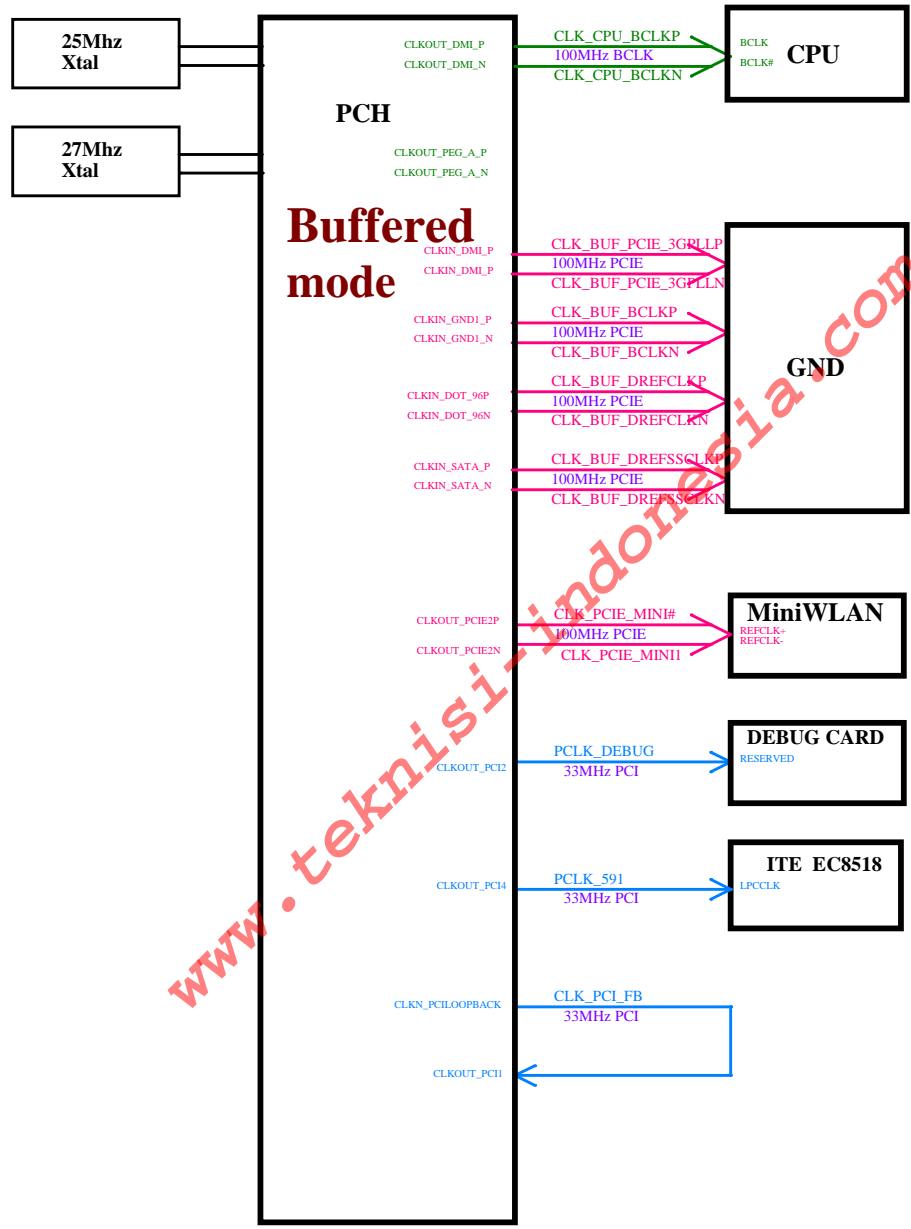
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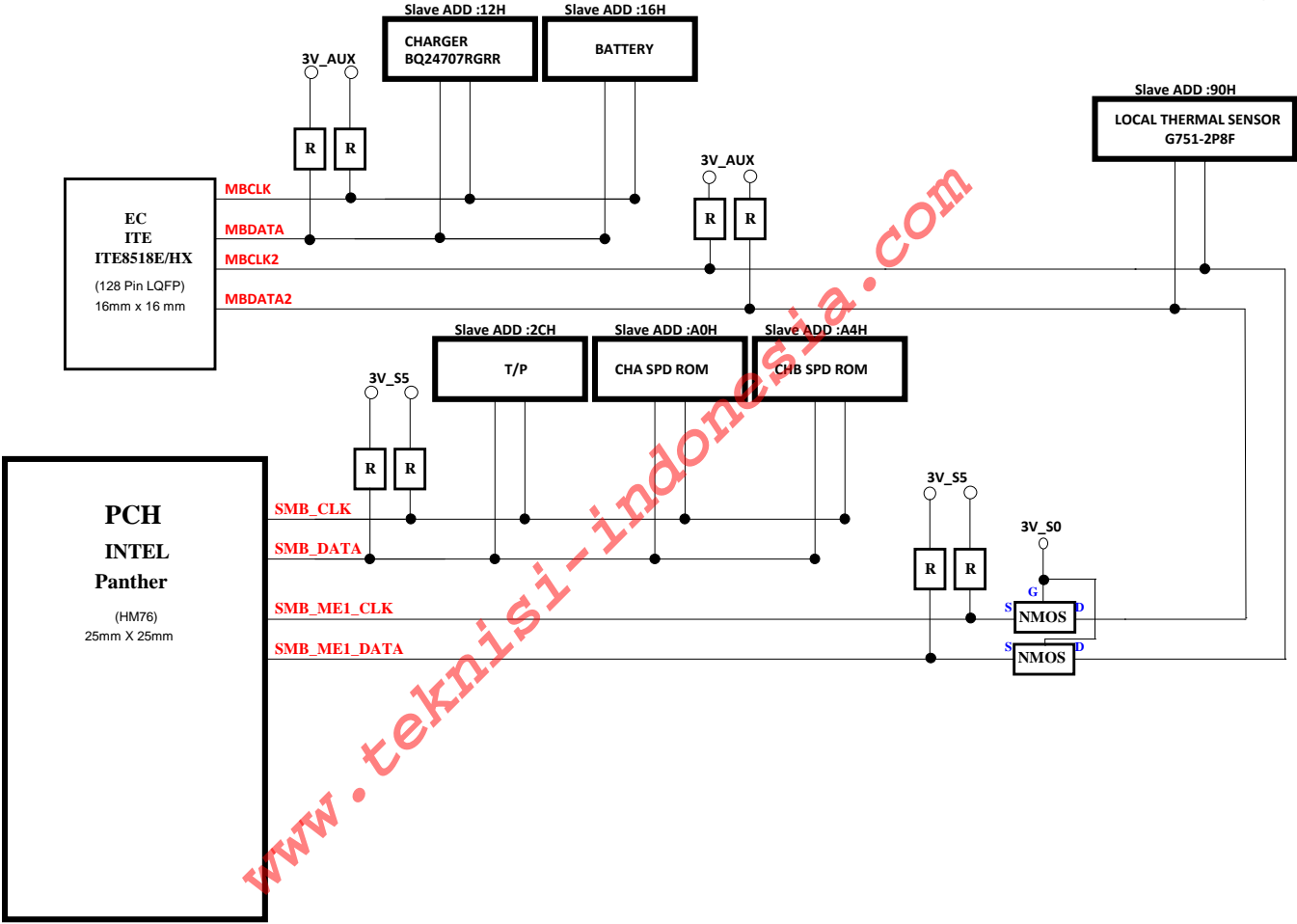
Power Tree Table



19V
3.42A



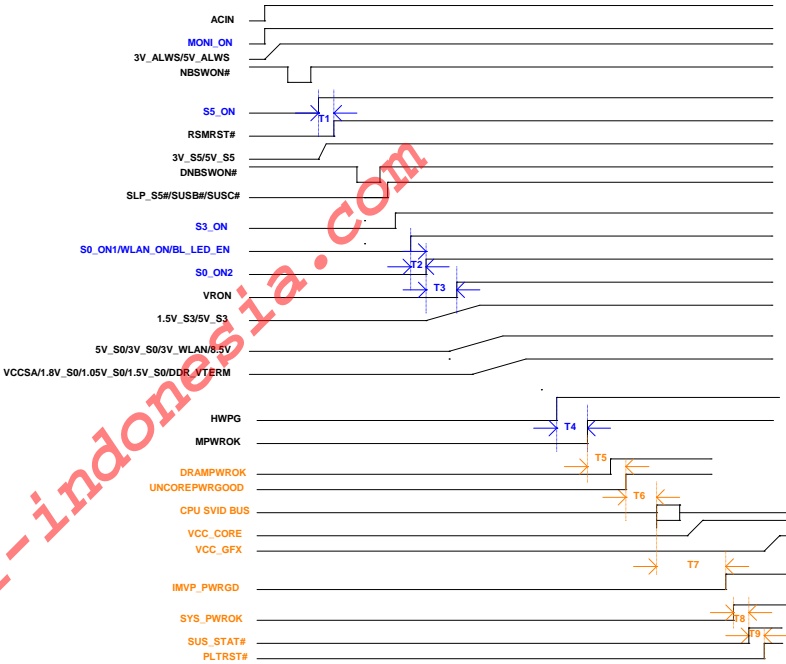




Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3VRTC	3V	ON	ON	ON	ON	ON	Adaptor in
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
3V_ALWS	5V	ON	ON	ON	ON	OFF	MONI_ON
5V_ALWS	3.3V	ON	ON	ON	ON	OFF	MONI_ON
5V_S5	5V	ON	ON	ON	ON	OFF	S5_ON
3V_S5	3V	ON	ON	ON	ON	OFF	S5_ON
12V_S5	12V	ON	ON	ON	ON	OFF	S5_ON
5V_S3	5V	ON	ON	ON	OFF	OFF	S3_ON
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	S3_ON
3V_WLAN	3V	ON	OFF	OFF	OFF	OFF	WLAN_ON
8.5V	8.5V	ON	OFF	OFF	OFF	OFF	BL_LED_EN
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON1
3V_S0	3V	ON	OFF	OFF	OFF	OFF	S0_ON1
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON2
1.8V_S0	1.8V	ON	OFF	OFF	OFF	OFF	S0_ON2
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON2
DDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	S0_ON2
VCCSA	0.8V	ON	OFF	OFF	OFF	OFF	HWPG_VTT
VCC_AXG	By VID	ON	OFF	OFF	OFF	OFF	VRON
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON

VZ7 SYSTEM POWER-ON SEQUENCE



System Power Sequence

EC Control:

T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)

T2: S0_ON1 TO S0_ON2 = 500us

T3: S0_ON2 TO VRON = 10ms

T4: HWPG TO MPWROK = 110ms (spec:mini 99ms)

Note:HWPG NEED TO BE HIGH at that time

System:

T5: MPWROK TO UNCOREPWROGOOD =2ms(Min)

T6: UNCOREPWROGOOD to SVID Packet =500us(Max)

T7: SVID Packet to IMVP_PWRGD =5ms(Max)

T8: SYS_PWROK to SUS_STAT# =1ms(Min)

T9:SUS_STAT# to PLTRST# =60us(Min)

Quanta Computer Inc.
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